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Abstract

Evaluation circuit and method for detecting and/or locating faulty data words in a data stream T_n

The evaluation circuit according to the invention comprises a first linear automaton circuit (L1) and also a second linear automaton circuit (L2) connected in parallel, each having a set of states z(t), which have a common input line for receiving a data stream T_n. The first linear automaton circuit (L1) and the second linear automaton circuit (L2) are designed such that a first signature (S1) and a second signature (S2), respectively, can be calculated. Situated downstream of the two linear automaton circuits (L1, L2) are respectively a first logic combination gate (XOR_{L1}) and a second logic combination gate (XOR_{L2}), which compare the signature (S1, S2) respectively calculated by the linear automaton circuit (L1, L2) with a predeterminable good signature and output a comparison value.

[Figure 5]